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Date: November 22, 2000

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09/717270
11/22/00

Sir:

Attached for filing is the patent application of:
Inventor: SUZUKI
Entitled: **ELECTRONIC CONTROL UNIT HAVING SINGLE NON-VOLATILE MEMORY FOR MULTIPLE CENTRAL PROCESSING UNITS AND DATA RETRIEVAL METHOD**
and including attachments as noted below:

☒ Declaration, ☒ Abstract
17 pages of specification and claims (including 20 numbered claims), and
5 sheets of accompanying drawings.
☒ Record & return the attached assignment to the undersigned.
☒ Priority is hereby claimed under 35 U.S.C 119 based on the following foreign applications, the entire content of which is hereby incorporated by reference in this application:

Application Number	Country	Day/Month/Year Filed
11-334277	JAPAN	25 November 1999
2000-325346	JAPAN	25 October 20000

, respectively.

☐ Certified copy(ies) of foreign application(s) is/are attached.
☐ Please amend the specification by inserting before the first line --This is a of PCT application , filed , the entire content of which is hereby incorporated by reference in this application.--
☐ Priority is hereby claimed under 35 U.S.C 120/365 based on the following prior PCT applications designating the U.S., the entire content of which is hereby incorporated by reference in this application:

Application Number	Country	Day/Month/Year Filed

☐ This application is based on the following prior provisional application(s):

Application No.	Filing Date

respectively, the entire content of which is hereby incorporated by reference in this application, and priority is hereby claimed therefrom.
☐ Please amend the specification by inserting before the first line: --This application claims the benefit of U.S. Provisional Application No. , filed , the entire content of which is hereby incorporated by reference in this application.--
☐ This application is entitled to "Small entity" status. ☐ "Small entity" statement attached.
☐ The Examiner's attention is directed to the prior art cited in the parent application by applicant and/or Examiner for the reasons stated therein.
☐ Preliminary amendment to claims (attached hereto), to be entered before calculation of the fee below.
☒ Also attached: **Information Disclosure Statement/ PTO-1449/ Two References**

FILING FEE IS BASED ON CLAIMS AS FILED LESS ANY HEREWITH CANCELED

Basic Filing Fee					$	710.00
Total effective claims	20	- 20 (at least 20) =	0	x $ 18.00	$	0.00
Independent claims	3	- 3 (at least 3) =	0	x $ 80.00	$	0.00
If any proper multiple dependent claims now added for first time, add $270.00 (ignore improper)					$	0.00
				SUBTOTAL	$	710.00
If "small entity," then enter half (1/2) of subtotal and subtract					-$(	0.00)
				SECOND SUBTOTAL	$	710.00
Assignment Recording Fee ($40.00)					$	40.00
				TOTAL FEE ENCLOSED	$	750.00

Any future submission requiring an extension of time is hereby stated to include a petition for such time extension.
The Commissioner is hereby authorized to charge any deficiency in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our **Account No. 14-1140.** A duplicate copy of this sheet is attached.

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Signature: Larry S. Nixon

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Our Ref.: 2018-354
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U.S. PATENT APPLICATION

Inventor(s): Takanao SUZUKI

Invention: ELECTRONIC CONTROL UNIT HAVING SINGLE NON-VOLATILE MEMORY FOR MULTIPLE CENTRAL PROCESSING UNITS AND DATA RETRIEVAL METHOD

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SPECIFICATION

ELECTRONIC CONTROL UNIT HAVING SINGLE NON-VOLATILE MEMORY FOR MULTIPLE CENTRAL PROCESSING UNITS AND DATA RETRIEVAL METHOD

CROSS REFERENCE TO RELATED APPLICATION

This application is based on and incorporates herein by reference Japanese Patent Applications No. 11-334277 filed November 25, 1999 and No. 2000-325346 filed October 25, 2000.

BACKGROUND OF THE INVENTION

This invention relates to an electronic control unit having a single non-volatile memory for multiple central processing units.

An electronic control unit (ECUs) for engines or vehicles use multiple central processing units (CPUs) and non-volatile memories such as electrically erasable programmable read-only memories (EEPROMs). The EEPROM is used to store therein, even when a power supply from a storage battery to the ECU is turned off, a vehicle export destination, a transmission type (manual or automatic), an engine type (natural aspirated or turbo charged), a vehicle identification code (VIN), malfunction information and the like.

United States Patent No. 4,896,263 teaches to use a single EEPROM for multiple CPUs so that the EEPROM is shared by the multiple CPUs. In this instance, as shown in Fig. 8, CPUs 11 and 12 are connected to each other through communication lines 14 and 15 and only the CPU 16 is connected to an EEPROM 13 through a signal line 16 in an ECU 10. The CPU 11 retrieves or reads out data from the EEPROM 13 and transmits the retrieved data to the

CPU 12 through the communication line 14, when initialization of software is effected. The CPU 11 receives all data of the CPU 12 to be written and stored in the EEPROM 13 through the communication line 15 and transmits the received data to the EEPROM 13.

In this ECU 10, as the EEPROM 13 is accessed via the CPU 11, the EEPROM access time of the CPU 11 increases and the communication data between the CPUs 11 and 12 increases. Further, in the initialization operation of the software, the CPU 12 is enabled to use the data of the EEPROM 13 only after the retrieved data are transmitted from the CPU 11, thus resulting in a time delay of using the retrieved data in the CPU 12.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an electronic control unit which is capable of efficiently accessing an electrically erasable programmable read-only memory and reducing communication data between multiple central processing units.

According to the present invention, an electronic control unit has multiple CPUs and a single non-volatile memory such as an EEPROM. The CPUs are programmed to directly receive data from the non-volatile memory without communication of retrieved data among the CPUs.

The CPUs may be programmed to generate respective data retrieving commands when the non-volatile memory is not being accessed for data retrieval by other CPUs. In this instance, the CPUs execute respective system register initialization

processing differently from each other after a start of power supply to the CPUs. Preferably, the system register initialization processing of a first CPU is divided while the system register initialization processing of a second CPU is not divided so that the data retrieving commands may be generated at different time points between the CPUs.

Alternatively, the CPUs may be programmed to generate a data retrieving command only from a first CPU and receive the retrieved data by both the first CPU and the second CPU at the same time.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description made with reference to the accompanying drawings. In the drawings:

Fig. 1 is a block diagram showing an electronic control unit according to a first embodiment of the present invention;

Figs. 2A and 2B are flow diagrams showing main routines of a first CPU and a second CPU used in the first embodiment;

Fig. 3 is a flow diagram showing a retrieval request processing in the first embodiment;

Fig. 4 is a flow diagram showing a receiving interrupt processing in the first embodiment;

Fig. 5 is a flow diagram showing a writing request processing in the first embodiment;

Fig. 6 is a flow diagram showing a time-synchronized processing in the first embodiment;

Figs. 7A and 7B are flow diagrams showing main routines of a first CPU and a second CPU according to a second embodiment of the present invention; and

Fig. 8 is a block diagram showing an electronic control unit according to a prior art.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention will be described with reference to various embodiments, in which an electronic control unit (ECU) is constructed with a pair of central processing units (CPUs) and a single non-volatile memory to control engine and vehicle operations.

(First Embodiment)

Referring first to Fig. 1, an ECU 10 has a first CPU 11, a second CPU 12 and a single electrically erasable programmable read-only memory (EEPROM) 13 which is a non-volatile type. The CPUs 11 and 12 are connected to each other through general ports or communication lines 14 and 15. The CPUs 11 and 12 are also connected to the EEPROM 13 through a chip select line 16 for data reading/writing, a clock line 17 and a serial communication interface (SCI) line 18 by sharing those lines. Here, the active level of the communication lines 14 and 15 which indicates that the EEPROM 13 is in use is defined with the low (L) level of the communication lines 14 and 15.

The CPUs 11 and 12 are programmed to execute various processing shown in Figs. 2A, 2B to Fig. 6. Data retrieving processing for retrieving data from the EEPROM 13 in the course of initialization of software is executed as shown in Figs. 2A

and 2B. When the ECU 10 is supplied with electric power, both CPUs 11 and 12 start to operate at almost the same time, and the CPUs 11 and 12 execute initializations in the main routines shown in Figs. 2A and 2B.

Specifically, as shown in Fig. 2A, the first CPU 11 initializes at step 101 only a system register of all of its system registers that is required to access the EEPROM 13. The CPU 11 retrieves or reads out only relevant data of all the stored data from the EEPROM 13 at step 102. The relevant data may be data which are relatively important to control a vehicle. Such data includes a vehicle export destination, a transmission type (manual or automatic), an engine type (natural aspirated or turbo charged), a vehicle identification code (VIN) and malfunction information. Thus, the initialization operation immediately after starting the power supply can be shortened and the access time to the EEPROM 13 can be shortened, by initializing only the relevant data with priority.

The CPU 11 then initializes the other system registers at step 103, and initializes application data at step 104, thus completing a sequence of initializations immediately after the start of power supply. The EEPROM data have already been retrieved at the time of initializing the application data. Thus, application processing can be appropriately changed by using the EEPROM data. When the other data in the EEPROM 13 become necessary in the course of execution of various normal controls, the CPU 11 retrieves other required data from EEPROM 13 at step 110.

The second CPU 12 initializes all of its system registers

at step 201 as shown in Fig. 2B, as opposed to the CPU 11 which initializes the system registers in two stages (steps 101 and 103). The CPU 12, in the similar manner as the CPU 11, retrieves only relevant data at step 202, initializes application data at step 203 and retrieves other data from EEPROM 13 at step 210. The relevant data retrieved at step 202 may be the similar data as retrieved at step 102.

As the CPU 12 initializes all the system registers at step 201, the timing of access to the EEPROM 13 is delayed. As a result, initialization can be effected efficiently because no waiting time for accessing the EEPROM 13 is necessitated.

Each EEPROM data retrieving processing of the first CPU 11 and the second CPU 12 is shown in Figs. 3 and 4, and is described particularly with respect to the first CPU 11. The routine of Fig. 3 is initiated each time step 102 or 110 of Fig. 2A (step 202 or 210 in Fig. 2B) is executed or each time an EEPROM data retrieval is requested by time-synchronized processing. The routine of Fig. 3 is designed to handle the case in which the accesses to the EEPROM 13 overlap at step 110 (step 210).

As shown in Fig. 3, the CPU 11 checks at step 301 whether the EEPROM 13 is being used or accessed by the second CPU 12. This determination may be made by checking whether the signal level of the communication line 15 is low (L). If the check result is YES, the processing jumps to step 307 and sets a return code (RC) to "BUSY" which indicates that the EEPROM data cannot be retrieved. If the check result is NO, the CPU 11 sets at step 302 the signal level of the communication line 14 to low (L) to

notify the CPU 12 that the EEPROM 13 is in use, so that the EEPROM 13 may be used for retrieving data. The CPU 11 then sets a retrieval command in a transmission register at step 303. The CPU 11 sets a retrieval mode at step 304 and allows a receiving interrupt at step 305. The CPU 11 finally sets at step 306 the return code to "OK" which indicates that the EEPROM data can be retrieved.

The CPU 11 initiates the routine of Fig. 4 upon receiving the data receiving interrupt from EEPROM 13. The CPU prohibits at step 401 receiving interrupts, and receives data from EEPROM 13 at step 402. The received data is copied from a register to a random access memory (RAM) in the CPU 11. The CPU 11 resets the mode to "NONE" at step 403, and resets the signal level of the communication line 14 to high (H) thus notifying the CPU 12 that the EEPROM 13 is in non-use, that is, the EEPROM data can be retrieved.

In the above operation, the check result at step 301 is YES without fail each time the routine of Fig. 3 is initiated in response to step 102 (step 202). As a result, the subsequent EEPROM data retrieving processing can be executed immediately.

Each EEPROM data writing processing of the first CPU 11 and the second CPU 12 is shown in Figs. 5 and 6, and is described particularly with respect to the first CPU 11. The routine of Fig. 5 is initiated each time an EEPROM data writing is requested by, for instance, time-synchronized processing.

As shown in Fig. 5, the CPU 11 checks at step 501 whether the EEPROM 13 is being used or accessed by the second CPU 12.

This determination may be made by checking the signal level of the communication line 16. If the check result is YES, the processing jumps to step 506 and sets a return code (RC) to "BUSY" which indicates that the EEPROM data cannot be written. If the check result is NO, the CPU 11 sets at step 502 the signal level of the communication line 14 to low (L) to notify the CPU 12 that the EEPROM 13 is in use so that the data may be written into the EEPROM 13. The CPU 11 then sets a writing command in a transmission register at step 503. The CPU 11 finally sets at step 506 the return code to "OK" which indicates that the EEPROM data can be written.

The CPU 11 initiates a time-synchronized routine of Fig. 6 upon receiving a writing interrupt at a predetermined interval. The CPU 11 checks at step 601 whether the mode is set to the writing mode. If the check result is YES, the CPU 11 further checks at step 602 whether the EEPROM 13 is busy, that is, the EEPROM 13 is in the writing command processing. If the check results at steps 601 and 602 are NO and YES, respectively, the routine ends. If the check result at step 602 is NO, the CPU 11 resets the mode to "NONE" at step 603 and returns the signal level of the communication line 14 to high (H) at step 604 to notify the CPU 12 that the EEPROM 13 has been set to non-use.

In the first embodiment, one CPU (for instance, CPU 11) checks at steps 301 and 501 whether the other CPU (for instance, CPU 12) is accessing the EEPROM 13, before accessing the EEPROM 13 for data retrieving or writing. It notifies the other CPU at steps 302 and 502 that it will access the EEPROM 13. After

completing the access to the EEPROM 13, it resets the notification of access at steps 404 and 604. With these notifications, the other CPU accesses directly the EEPROM 13 without data communication between the CPUs. Thus, the access time can be shortened and the amount of data communicated between the CPUs can be reduced remarkably.

Further, the CPUs 11 and 12 are programmed to access the EEPROM 13 at different time points in the course of respective initialization operations. As a result, the access wait time can be eliminated and the initialization operation can be completed in a short period of time.

Still further, only the relevant data of high priority such as the vehicle information and malfunction information are retrieved first in the initialization operation of the ECU 10, and other data of low priority are retrieved later when requested in the normal control operation other than the initialization operation. As a result, the initialization operation of the CPUs 11 and 12 can be shortened further.

In addition, the EEPROM data are retrieved before the initialization of the application data. As a result, the processing can be switched from one to another with reference to the EEPROM data in the course of executing the application processing.

The first embodiment may be modified in various ways. For instance, the use or non-use of the EEPROM 13 may be checked by chip-select state indicated by the signal level of the chip select interface (SCI) line 18 without connecting the first CPU 11 and

the second CPU 12 via the communication lines (ports) 14 and 15. Further, the EEPROM data may be shared by more than two CPUs. In this instance, it is preferred to divide the initialization processing of system registers and the initialization processing of application data of each CPU so that each CPU executes the EEPROM data retrieval at different time points from other CPUs.

(Second Embodiment)

In a second embodiment, the first CPU 11 and the second CPU 12 are programmed as shown in Figs. 7A and 7B, respectively, so that EEPROM data, which are to be shared by each CPU, are retrieved at the same time from the EEPROM 13 in the initialization processing thereby to shorten the time period required for the initialization operation. In the second embodiment, the first CPU 11 and the second CPU 12 are used as a master CPU and a slave CPU, respectively. When the power supply to the ECU 10 is started, the CPUs 11 and 12 start executing the respective routines.

As shown in Fig. 7A, the first CPU 11 initializes its system registers at step 701. The CPU 11 then transmits a retrieving command to the CPU 12 and the EEPROM 13 through the SCI line 18 (Fig. 1) at step 702, so that EEPROM data which are shared by both CPUs 11 and 12 are retrieved. The retrieving command identifies which one of the shared data (address) is to be retrieved. The CPU 11 receives through the SCI line 18 the EEPROM data retrieved from the EEPROM 13 in response to the shared data retrieving command. The CPU 11 further transmits a retrieving command and receives EEPROM data at steps 704, 705 and the like repeatedly in the similar manner as at steps 702 and 703.

After the above retrieval of the EEPROM data to be shared, the CPU 11 then retrieves at step 711 individual data from the EEPROM 13 to be used individually by the CPU 11. The CPU 11 then initializes the application data at step 712 and retrieves other data from the EEPROM 13 at step 713 when requested in the course of its normal control processing.

As shown in Fig. 7B, the second CPU 12 initializes its system registers at step 801. The CPU 12 then receives at step 802 the shared data retrieving command which the CPU 11 issued at step 702 through the SCI line 18 (Fig. 1). The CPU 12 receives at step 803 through the SCI line 18 the EEPROM data retrieved from the EEPROM 13 in response to the retrieving command of the CPU 11. The CPU 12 further receives the retrieving command and receives EEPROM data at steps 804, 805 and the like repeatedly in the similar manner as at steps 802 and 803.

After the above retrieval of the EEPROM data to be shared, the CPU 12 then retrieves at step 811 individual data from the EEPROM 13 to be used individually by the CPU 12. The CPU 12 then initializes the application data at step 812 and retrieves other data from the EEPROM 13 at step 813 when requested in the course of its normal control processing.

According to the second embodiment, each shared data transmitted from the EEPROM 13 in response to the shared data retrieving commands of one CPU 11 is received by both CPUs 11 and 12 at the same time. As the CPU 12 receives each shared data retrieval command from the CPU 11 through the SCI line 18, the CPU 12 can recognize which one of the shared data it will receive.

When the individual data are retrieved one by one after the retrieval of the shared data, the retrieval of all data required for the initialization operations of the CPUs 11 and 12 is completed. In each of the CPUs 11 and 12, all the retrieved data are stored in corresponding addresses of the respective RAMs.

Thus, each data to be shared by the CPUs 11 and 12 is retrieved in one retrieval operation, thereby shortening the initialization processing. As the shared data retrieval is started immediately after the initializations of the system registers in the CPUs 11 and 12, the timing of data retrieving operations of the CPUs 11 and 12 can be synchronized. As a result, the shared data is ensured to be received by both CPUs 11 and 12 at the same time.

The second embodiment may also be modified in various ways. For instance, the synchronization of operations between the CPUs 11 and 12 may be effected based on the signal level of the chip select interface (CSI) line 18 when the operating frequency of the CPUs 11 and 12 are different from each other, in place of starting the shared data retrieving immediately after the initialization of the system registers. Further, in case that the EEPROM data are shared by more than two CPUs, the ECU 10 may be constructed so that one of the CPUs issues the data retrieving command and transmits the same to the other CPUs.

The present invention should not be limited to the disclosed embodiments and modifications, but may be implemented in many other ways without departing from the spirit of the invention.

WHAT IS CLAIMED IS:

1. An electronic control unit comprising:

a plurality of CPUs;

a single non-volatile memory; and

communication ports connecting the CPUs and the non-volatile memory one another,

wherein a first one of the CPUs is programmed to check whether a second one of the CPUs is accessing the non-volatile memory before accessing the non-volatile memory, send to the second CPU a notification that the first CPU will access the non-volatile memory when a check result indicates that the second CPU is not accessing the non-volatile memory, and stops the notification to the second CPU after completing an access to the non-volatile memory.

2. The electronic control unit as in claim 1, wherein:

the CPUs are connected through the ports; and

the first CPU is programmed to set a signal level of the port to a level indicative of its accessing when starting to access the non-volatile memory.

3. The electronic control unit as in claim 1, wherein:

the CPUs are programmed to execute respective accessing to the non-volatile memory at different time points in initialization operations executed when a power supply to the CPUs is started.

4. The electronic control unit as in claim 3, wherein:

the first CPU is programmed to execute initialization operations of system registers thereof in divided manner thereby to differentiate the time points of the initialization operations from that of the second CPU.

5. The electronic control unit as in claim 3, wherein:

the CPUs are programmed to retrieve only specified high-priority data from the non-volatile memory in the respective initialization operations, and retrieves other low-priority data from the non-volatile memory only when required after completion of the initialization operations.

6. An electronic control unit comprising:

a plurality of CPUs;

a single non-volatile memory; and

communication ports connecting the CPUs and the non-volatile memory one another,

wherein a first one of the CPUs is programmed to transmit a data retrieving command, and the first CPU and the second CPU are programmed to receive at the same time same data from the non-volatile memory retrieved in response to the data retrieving command of the first CPU thereby to share the same retrieved data.

7. The electronic control unit as in claim 6, wherein the second CPU is programmed to receive the data retrieving command from the first CPU.

8. The electronic control unit as in claim 6, wherein:

the first CPU and the second CPU are programmed to be synchronized with each other and receive the same data from the non-volatile memory after being synchronized.

9. The electronic control unit as in claim 6, wherein:

the first CPU and the second CPU are programmed to retrieve respective individual data other than the same data separately from each other after receiving the same data.

10. The electronic control unit as in claim 6, wherein:

only the first CPU is programmed to transmit the data retrieving command as a master CPU, and the second CPU is programmed to receive the data retrieving command before receiving the same data from the non-volatile memory.

11. A data retrieving method in an electronic control unit having a first CPU, a second CPU and a single non-volatile memory, the method comprising the steps of:

generating a data retrieving command from the first CPU and notifying the second CPU that the first CPU transmits the data retrieving command;

retrieving data from the non-volatile memory in response to the data retrieving command; and

receiving the retrieved data by at least the first CPU directly from the non-volatile memory.

12. The method as in claim 11, further comprising the step of:

initializing a system register of the first CPU before generating the data retrieving command, the system register being associated with an access operation of the first CPU to the non-volatile memory; and

initializing other system registers of the first CPU after receiving the data from the non-volatile memory by the first CPU.

13. The method as in claim 12, further comprising the steps of:

initializing all system registers of the second CPU before generating a data retrieving command from the second CPU, so that data retrieving operations of the first CPU and the second CPU occurs at different time points.

14. The method as in claim 11, further comprising the step of:

generating a data retrieval command from the second CPU by checking that the first CPU is not accessing the non-volatile memory,

wherein the first CPU and the second CPU are capable of directly retrieving data from the non-volatile memory, respectively, independently of each other.

15. The method as in claim 14, wherein:

the first CPU and the second CPU retrieves only predetermined high-priority data from the non-volatile memory.

16. The method as in claim 11, wherein:

the data retrieving command is generated only by the first CPU; and

the retrieved data is received by both the first CPU and the second CPU at the same time.

17. The method as in claim 16, wherein:

the retrieved data is limited to data that are shared by both of the first CPU and the second CPU.

18. The method as in claim 17, further comprising the step of:

generating individual data retrieving commands from the first CPU and the second CPU to retrieve individual data other than the data to be shared from the non-volatile memory, respectively, after the data receiving step.

19. The method as in claim 16, further comprising the step of:

initializing system registers of the first CPU and the second CPU at the same time immediately after a start of power supply to the first CPU and the second CPU before generating the data retrieving command from the first CPU.

20. The method as in claim 19, further comprising the step of:

generating individual data retrieving commands from the first CPU and the second CPU to retrieve individual data other than the data to be shared from the non-volatile memory, respectively, after the data receiving step.

ABSTRACT OF THE DISCLOSURE

An electronic control unit for engines or vehicles has multiple CPUs and a single non-volatile memory such as an EEPROM. The CPUs are programmed to directly receive data from the EEPROM. The CPUs may be programmed to generate respective data retrieving commands when the EEPROM is not being accessed for data retrieval. In this instance, the CPUs execute respective system register initialization processing differently from each other after a start of power supply. For instance, the system register initialization processing of a first CPU is divided while the system register initialization processing of a second CPU is not divided. Alternatively, the CPUs may be programmed to generate a data retrieving command only from the first CPU and receive the retrieved data by both the first CPU and the second CPU at the same time.

FIG. 1

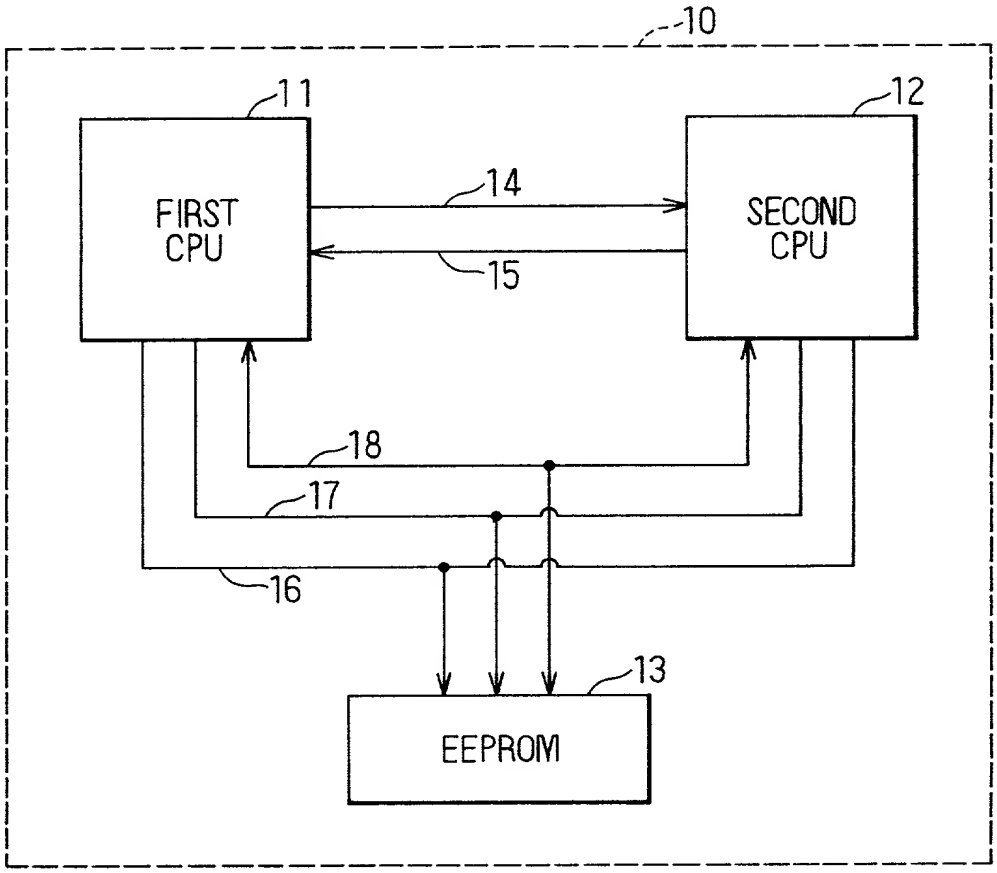


FIG. 8 PRIOR ART

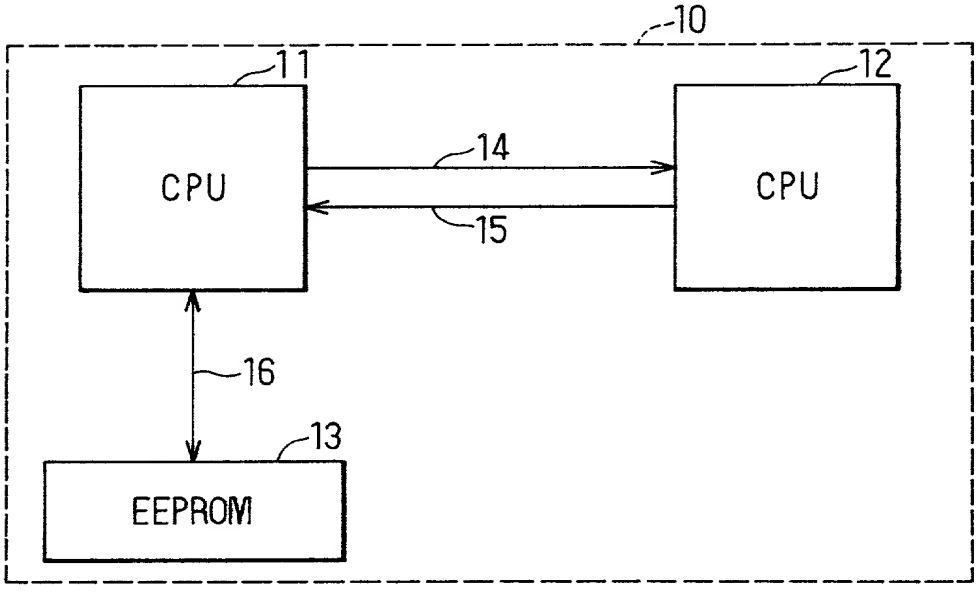


FIG. 2A

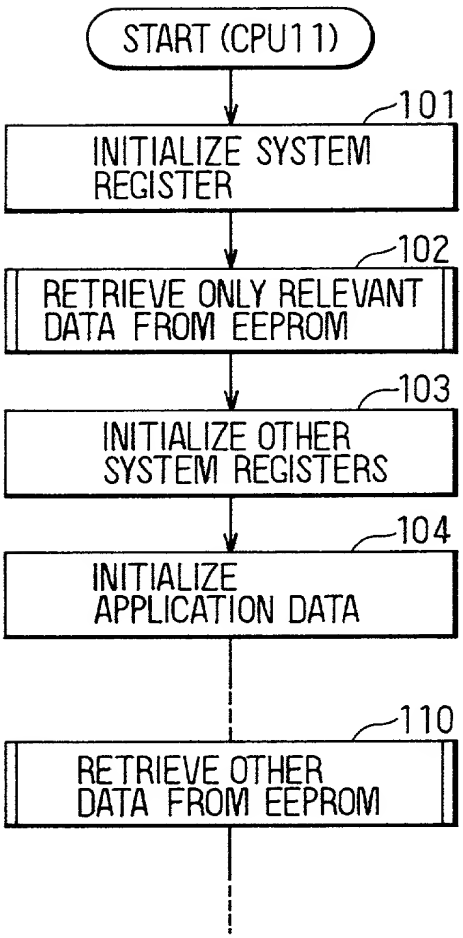

START (CPU11)
101
INITIALIZE SYSTEM REGISTER
102
RETRIEVE ONLY RELEVANT DATA FROM EEPROM
103
INITIALIZE OTHER SYSTEM REGISTERS
104
INITIALIZE APPLICATION DATA
110
RETRIEVE OTHER DATA FROM EEPROM

FIG. 2B

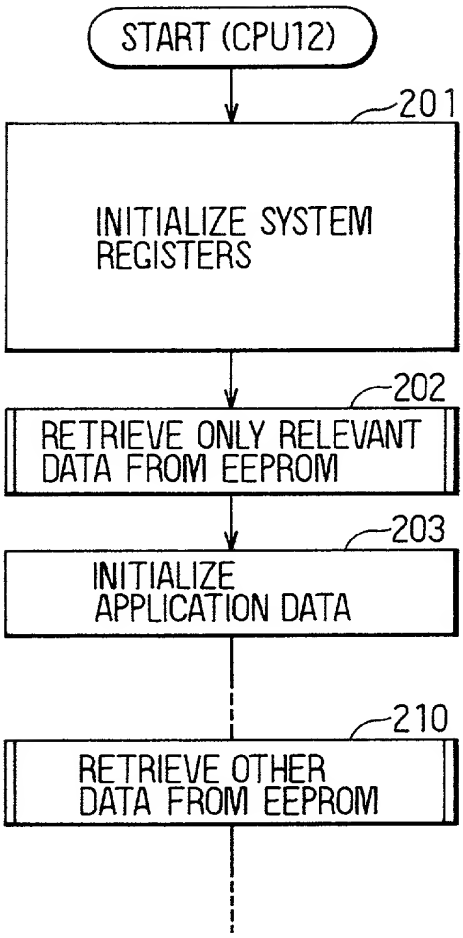

START (CPU12)
201
INITIALIZE SYSTEM REGISTERS
202
RETRIEVE ONLY RELEVANT DATA FROM EEPROM
203
INITIALIZE APPLICATION DATA
210
RETRIEVE OTHER DATA FROM EEPROM

FIG. 3

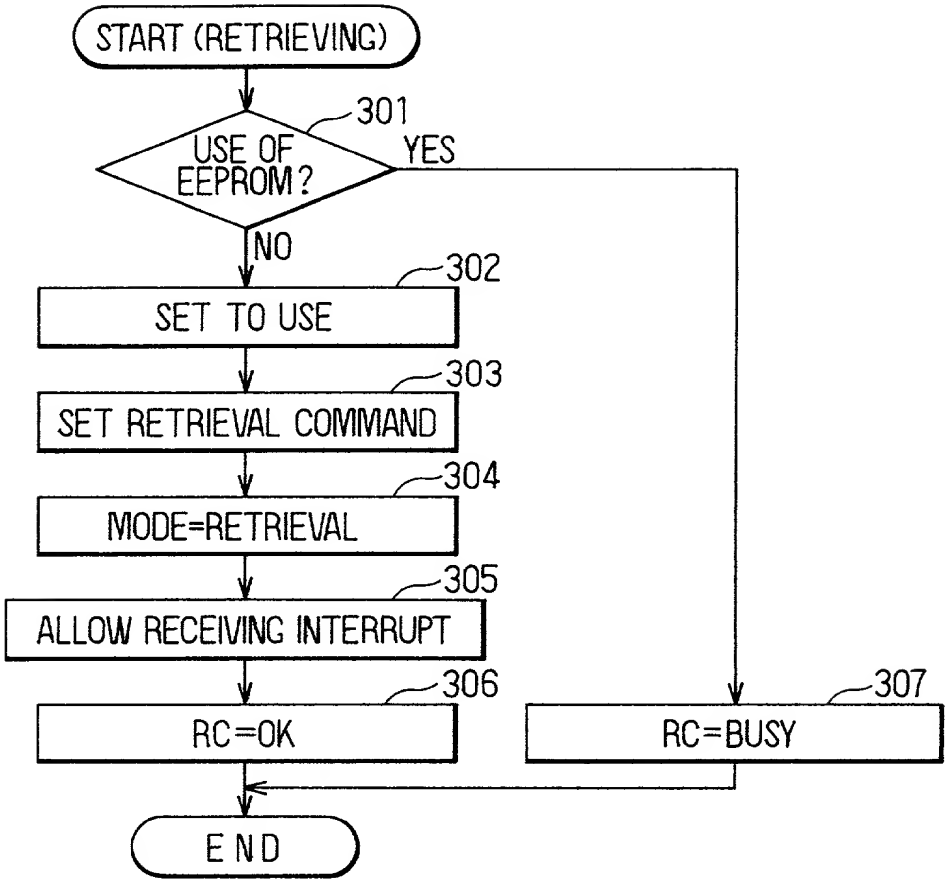

START (RETRIEVING)
301
USE OF EEPROM?
YES
NO
302
SET TO USE
303
SET RETRIEVAL COMMAND
304
MODE=RETRIEVAL
305
ALLOW RECEIVING INTERRUPT
306
RC=OK
307
RC=BUSY
END

FIG. 4

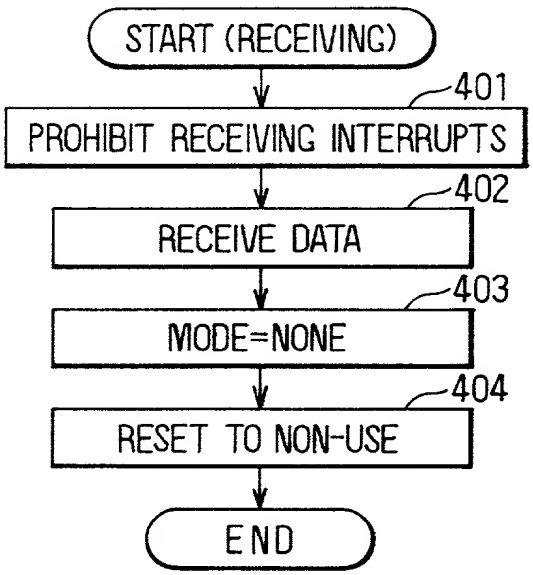

START (RECEIVING)
401
PROHIBIT RECEIVING INTERRUPTS
402
RECEIVE DATA
403
MODE=NONE
404
RESET TO NON-USE
END

FIG. 5

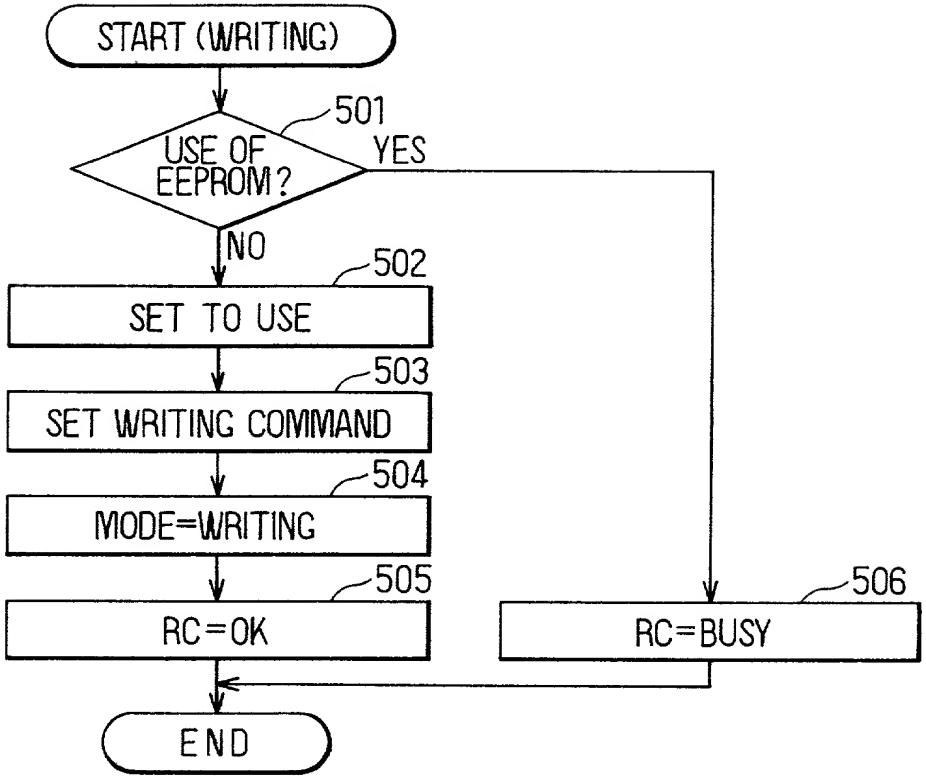

START (WRITING)
501
USE OF EEPROM?
YES
NO
502
SET TO USE
503
SET WRITING COMMAND
504
MODE=WRITING
505
RC=OK
506
RC=BUSY
END

FIG. 6

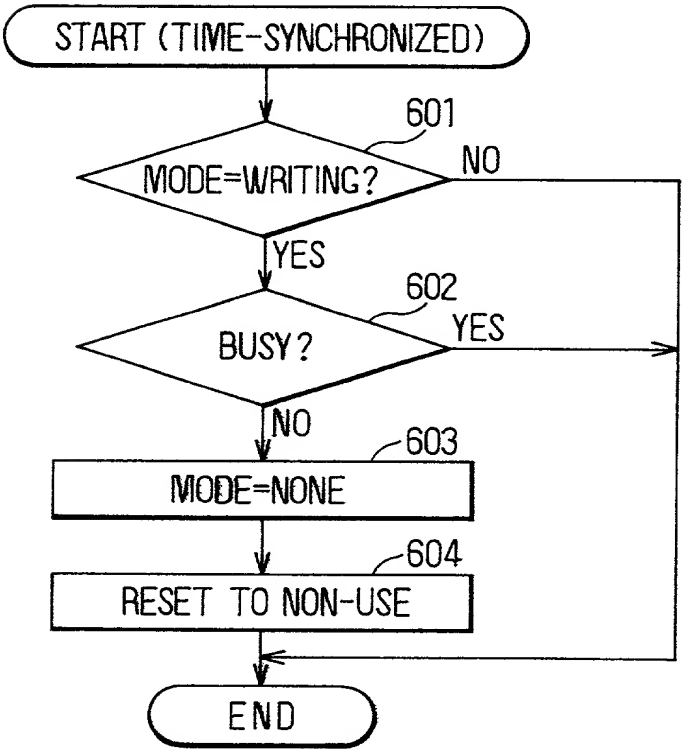

START (TIME-SYNCHRONIZED)
601
MODE=WRITING?
NO
YES
602
BUSY?
YES
NO
603
MODE=NONE
604
RESET TO NON-USE
END

FIG. 7A

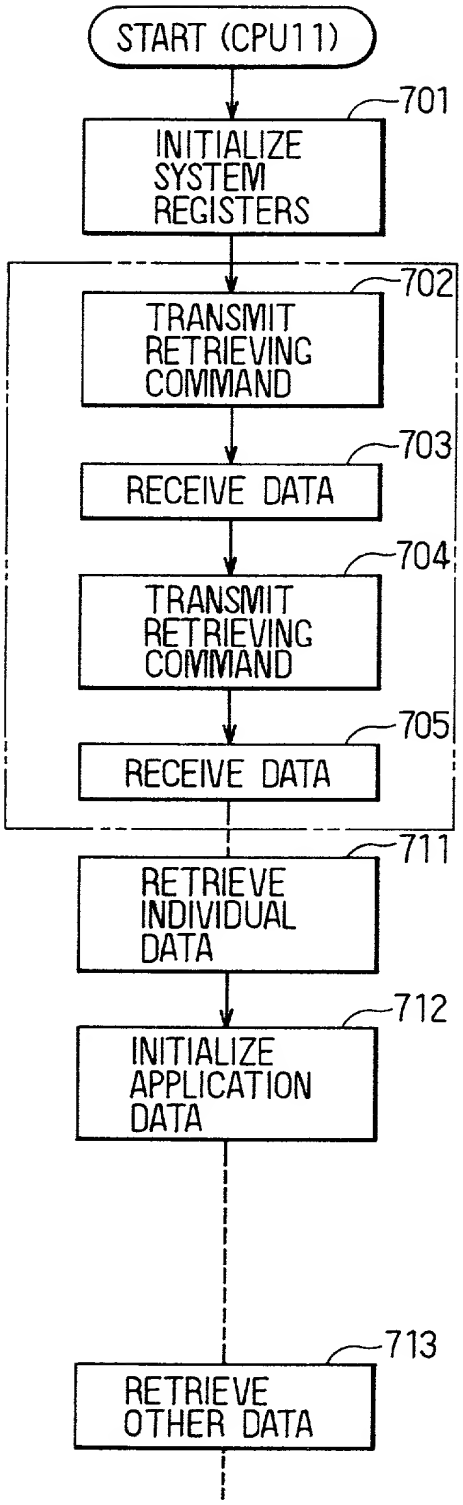
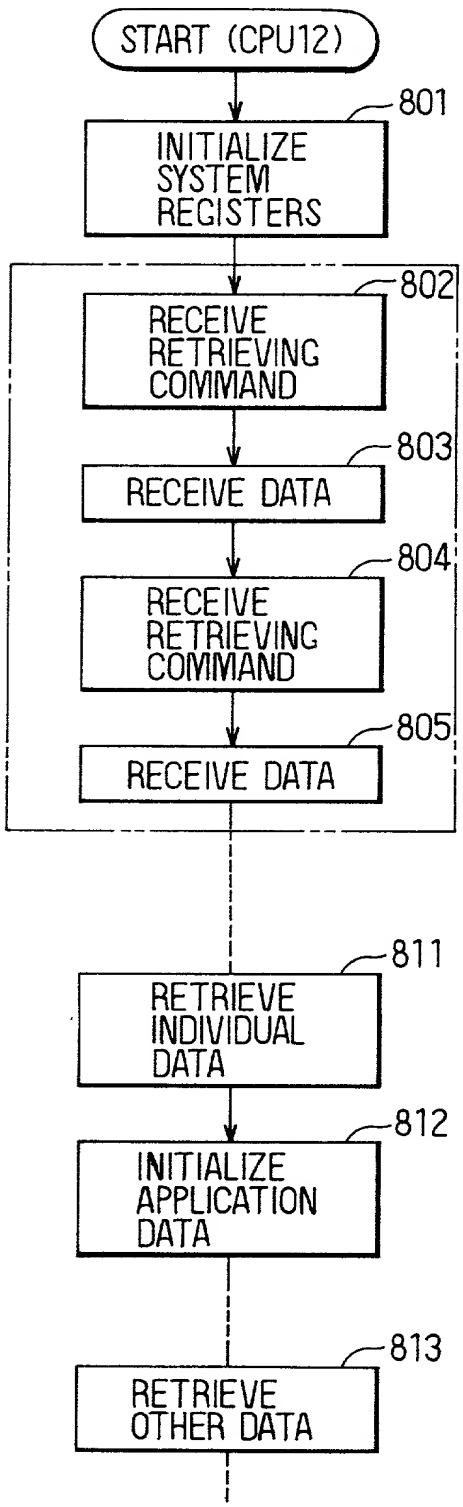

START (CPU11)
701
INITIALIZE SYSTEM REGISTERS
702
TRANSMIT RETRIEVING COMMAND
703
RECEIVE DATA
704
TRANSMIT RETRIEVING COMMAND
705
RECEIVE DATA
711
RETRIEVE INDIVIDUAL DATA
712
INITIALIZE APPLICATION DATA
713
RETRIEVE OTHER DATA

FIG. 7B


START (CPU12)
801
INITIALIZE SYSTEM REGISTERS
802
RECEIVE RETRIEVING COMMAND
803
RECEIVE DATA
804
RECEIVE RETRIEVING COMMAND
805
RECEIVE DATA
811
RETRIEVE INDIVIDUAL DATA
812
INITIALIZE APPLICATION DATA
813
RETRIEVE OTHER DATA

Declaration and Power of Attorney for Patent Application
特許出願宣誓書及び委任状
Japanese Language Declaration
日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者(下記の氏名が一つの場合)もしくは最初かつ共同発明者であると(下記の名称が複数の場合)信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ELECTRONIC CONTROL UNIT HAVING SINGLE NON-VOLATILE MEMORY FOR MULTIPLE CENTRAL PROCESSING UNITS AND DATA RETRIEVAL METHOD

上記発明の明細書(下記の欄で×印がついていない場合は、本書に添付)は、

the specification of which is attached hereto unless the following box is checked:

☐ _____に提出され、
米国出願番号または特許協力条約国際出願番号を
_____とし、
(該当する場合)_____に訂正されました。

☐ was filed on_____
as United States Application Number or PCT International Application Number_____
and was amended on _____
(if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基き下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約365(a)項に基く国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

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Japanese Language Declaration
(日本語宣言書)

Prior Foreign Application(s) 外国での先行出願			Priority Not Claimed (優先権主張なし)
1. 11-334277	Japan	25/NOVEMBER/1999	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	
2. 2000-325346	Japan	25/OCTOBER/2000	☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	
3.			☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	
4.			☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	
5.			☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	
6.			☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	
7.			☐
(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	

☐ Additional Foreign Application(s) is(are) listed on the attached sheet which is incorporated herein by reference.

私は、第３５編米国法典１１９条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)

(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(c)に基く権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

Application No. (出願番号)	Filing Date (出願日)	Status : (現況)	Patented, (特許許可済)、	Pending, (係属中)、	Abandoned (放棄済)

Japanese Language Declaration
(日本語宣言書)

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私は、私自身の知識に基いて本宣言書中で私が行う表明が真実であり、かつ私の入手した情報と私の信じるところに基く表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基き、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行えば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

委任状： 私は下記の発明者として、本出願に関する一切の手続を米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。(弁護士、または代理人の氏名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

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国籍 (Citizenship)	Japan
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第二共同発明者 (Full name of second joint inventor)	
発明者の署名 (Inventor's Signature)	
日付 (Date)	
住所 (Residence)	
国籍 (Citizenship)	
私書箱 (Post Office Address)	

☐ Additional Inventor(s) is (are) listed on the attached sheet which is incorporated herein by reference.